a second polycrystalline silicon layer overlying the first polycrystalline silicon layer and the first substrate region.

39. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region [, including a field oxide region,] overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the [field oxide and gate] oxide [regions] region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the [field] oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the etch stop layer and the first substrate region.

40. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region [, including a field oxide region,] overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the [field oxide and gate] oxide [regions] region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the [field] oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the etch stop layer and the first substrate

region, the upper surface of the second polycrystalline silicon layer being substantially planar and aligned with the upper surface of the first polycrystalline silicon layer adjacent an interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer such that the interface has no horizontal component.

41. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

a field oxide region overlying at least a portion of the second substrate region;

a gate oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the field oxide and gate oxide regions but not the first substrate region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the [field] oxide regions [region];

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

42. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region [, including a field oxide region,] overlying at least a portion of the second substrate region;

a polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the [field] oxide region;

a polycrystalline silicon plug overlying the first substrate region and having the upper

surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and

a photoresist mask of material resistant to polycrystalline silicon etching overlying the polycrystalline silicon plug and an adjacent portion of the first polycrystalline layer surrounding the polycrystalline silicon plug thereby defining an electrical interconnect.

43. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region [, including a field oxide region,] overlying at least a portion of the second substrate region;

a polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the [field] oxide region;

a polycrystalline silicon plug overlying the first substrate region and having an upper surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and

a photoresist mask overlying the polycrystalline silicon plug to define an electrical interconnect.

45. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region [, including a field oxide region,] overlying at least a portion of the second substrate region;

a polycrystalline silicon plug overlying the first substrate region; and

a polycrystalline silicon layer overlying a portion of the oxide region adjacent the

polycrystalline silicon plug, but not the first substrate region, the polycrystalline silicon layer having a thickness selected such that a lowest upper surface of the polycrystalline silicon layer is higher than a highest upper surface of the [field] oxide region, the polycrystalline silicon layer also having an upper surface thereof in the region adjacent the polycrystalline silicon plug aligned with an upper surface of the polycrystalline silicon plug such that the vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component.

48. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region [including a field oxide region] overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the [field] oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium layer overlying the etch stop layer and the polycrystalline silicon plug layer.

49. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region [including a field oxide region] overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate

region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the [field] oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug;

a titanium layer overlying the etch stop layer; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug layer.

50. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region [, including a field oxide region,] overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the [field] oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug layer.

51. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a buried contact region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region [, including a gate oxide region,] overlying at least a portion of the

second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the [field] oxide region;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug.

52. (Amended) An intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region [, including a field oxide region,] overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer partially overlying the oxide region adjacent the first substrate region but not overlying the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the [field] oxide region;

a polycrystalline silicon plug overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug; and

a titanium silicide etch stop layer overlying the polycrystalline silicon plug.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on June 5, 2002, and the references cited therewith.

Claims 38 - 43, 45 and 48 - 52 are amended, claims 46, 66 and 67 are canceled, and no claims are added; as a result, claims 38 - 45, 47 - 52, 54 - 65 and 68 -79 are now pending in this application.